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Title:

SIGNAL PROCESSING SYSTEM FOR REDUCING POWER CONSUMPTION

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LOW POWER AUDIO PROCESSOR

Field of the Invention

The present invention relates generally to an audio signal processor, and, more particularly, to an audio signal processor having a plurality of sub-processing units which are only driven when currently needed for processing.

Background of the Invention

A conventional audio processor or signal processor digitally processes an application program by using a signal processing unit, which leads the whole signal processing unit to be driven at every flow, causing power consumption of the processor to be very high. Especially, when a high performance program is processed at a high frequency, unessential parts of the hardware are driven, and more power is consumed.

Summary of the Invention

According to a preferred embodiment of the invention, a low power audio processor is provided that comprises: a bit stream processing unit for bit processing an applied audio stream into a bit processed audio stream, and for decoding the bit processed audio stream to have a format conducive to digital signal processing. A digital signal processing unit is also included for digital signal processing the decoded bit processed audio stream from the bit stream processing unit to develop a digital signal processed audio stream. The audio processor further includes a post processing unit for receiving the digital signal processed audio stream from the digital signal processing unit to develop final audio data. A host interface unit is included for interfacing with an external device to provide an audio parallel stream received from the external device to the bit stream processing unit. A power control unit is included for determining the power state for each of the bit stream processing unit, the digital signal processing unit, and the post processing unit in response to (1) a request signal and an acknowledge signal between the digital signal processing unit and the post processing unit, (2) a power down signal and (3) a

source clock, the power control unit outputting a determined power state as a power mode signal. There is also an internal clock signal generator unit for generating clock signals in response to the power mode signal, each of the clock signals corresponding to a respective one of the bit stream processing unit, the digital signal processing unit, and the post processing unit.

Brief Description of the Drawings

The following description of preferred embodiments refers to the accompanied drawings, in which:

Fig. 1 is a block diagram of an exemplary audio processor constructed in accordance with the teachings of the present invention;

Fig. 2 shows an internal state diagram of the PMU of Fig. 1; and

Fig. 3 offers an internal block diagram of the internal clock signal generator of Fig. 1.

Detailed Description

Fig. 1 is a block diagram of an exemplary audio processor constructed in accordance with the teachings of the present invention. As shown in Fig. 1, the disclosed audio processor comprises a bit stream processing (BSP) unit 100 for bit processing of an applied audio stream to compress the audio stream. The BSP unit 100 also decodes the bit processed audio stream to a format amenable to digital signal processing. A digital signal processing (DSP) unit 110 receives the decoded data in the digital signal processing format from the BSP unit 100 and performs digital signal processing by using a digital signal processing algorithm. A post processing unit 120 receives audio data from the DSP unit 110 and performs further post processing, such as equalizing processing, and outputs final audio data.

A host interface unit 130 is also included to interface with an external device through a parallel bus and/or a serial bus. The host interface unit 130 transmits an audio stream from an external device through the parallel bus to the BSP unit 100. The audio processor also includes a power control unit (PMU) 140 for determining idle states for each unit. The PMU 140 accomplishes this power control by using a

request signal and an acknowledge signal between the DSP unit 110 and the post processing unit 120. These signals are generated in response to a power down signal PWRDN from outside and a source clock SOURCE_CLOCK to output the determined power state as a power mode signal.

The audio processor further includes an internal clock signal generator 150 for generating clock signals that correspond to each unit in response to the power mode signal to output each of the clock signals to the corresponding units.

A program memory is also included in the audio processor, which is coupled to the BSP unit 100, the DSP unit 110 and the post processing unit 120. The program memory 160 is driven by a memory clock MEM_CLK from the internal clock signal generator 150. The memory clock is driven when the BSP unit 100, the DSP unit 110 and the post processing unit 120 perform processing.

Still referring to Fig. 1, the BSP unit 100 performs the bit processing for the audio stream, analyzes the compressed data, and then converts the format of the compressed data to a format for digital signal processing. The DSP unit 110 performs typical audio algorithm processing and the post processing unit 120 outputs real time audio data. Therefore, the request signal and the acknowledge signal are transferred among the BSP unit 100, the DSP unit 110 and the post processing unit 120 to perform the processing sequentially in order of the BSP unit 100, the DSP unit 110 and the post processing unit 120, which confirms the start and end of processing that is performed at each unit. The request signal and the acknowledge signal are applied to the input of the PMU 140.

Since the idle state of each unit can be recognized from the request signals and the acknowledge signals, the PMU 140 specifies the power state based upon the request signals and the acknowledge signals. The PMU 140 then outputs the specified power state as the mode signal.

The internal clock signal generator 150 generates clock signals BSP_CLK, DSP_CLK, POST_CLK, each of which is applied to one of the corresponding units 100, 110 and 120, depending on the mode signal from the PMU 140. The clock signal generator 150 also generates the memory clock MEM_CLK to enable the memory 160 when one of the units 100, 110 and 120 performs a processing

operation in response to a corresponding clock signal from the internal clock signal generator 150.

Fig. 2 shows an internal state diagram for the PMU 140 of Fig. 1. As shown in Fig. 2, the PMU 140 has three states; standby state, run state and power off state.

The standby state is a default state after reset. In this state, the internal clock signal generator 150 and the host interface unit 130 operate with a programmable clock of ½ of the source clock and the other processing units remain in a static state.

The run state is a state in which the host interface unit 130 performs parameter setup before a run command that is generated at the host interface unit 130. The state of each unit is also monitored to perform clock masking. During this state, the fundamental clock remains at ½ of the source clock and is divided by one, two or four as appropriate for the driven module.

Finally, when a power down pin is activated at the standby state, the state transits to the power off state in which the source clock becomes DC.

In other words, when processing is required during the standby state, (i.e., idle state), the run command is generated to transit to the run state. After that, a standby command is generated to transit to the standby state when the processing is ended. And, the standby state can transit to the power off state in which power is turned off through the external power down pin. Therefore, power consumption is reduced significantly.

Fig. 3 offers a block diagram of the internal clock signal generator 150 of Fig. 1. The internal clock generating means 150 includes a multiplexer 200 for selectively outputting one of a DC level and the source clock in response to the power down signal PWRDN. A divider 210 is included for dividing the output of the multiplexer 200 by one, two or four, and three multiplexers 220, 230 and 240. Each of the three multiplexors selects one of the corresponding clock signals applied from the branch 210 and the DC level in response to the idle state of the corresponding processing unit to output the selected signal to the corresponding processing unit.

Referring to Fig. 3, depending on the power state specified at the PMU 140, the internal clock signal generator 150 provides separate clock signals to the corresponding units.

The multiplexer 200 blocks input from the clock by selecting the DC instead of the source clock SOURCE_CLOCK during a power off state (identified by the power down signal PWRDN). It outputs the source clock SOURCE_CLOCK in all other states. The branch 210 branches the source clock SOURCE_CLOCK depending on the power mode to generate the clock signals for each unit.

After that, depending on the idle state of each processing unit, the clock signal branched at the branch 210 is applied to the BSP unit 100, the DSP unit 110 and the post processing unit 120.

On the other hand, data processed at each of the processing units is temporarily stored at the memory device 160. As flow occurs sequentially, data processed at the BSP unit 100 is the input of the DSP unit 110. Data that has then undergone digital signal processing at the DSP unit 110 is the input of the post processing unit 120. Therefore, the memory is driven by not only one of the processing units but by two of the processing units. Because the clock signal MEM_CLK for driving the memory 160 cannot be used commonly with the clock for each unit, the memory clock MEM_CLK is separately generated by a logic device 250 (i.e., an OR gate operating the clock signal BSP_CLK from the BSP unit 100, the clock signal DSP_CLK from the DSP unit 110, and the clock signal POST_CLK from the post processing unit 120) in the internal clock signal generator 150 as shown in Fig. 3.

As described above, the disclosed audio processing unit is subdivided functionally into the bit stream processing unit 100, the digital signal processing unit 110, and the post processing unit 120 for audio signal processing. Also, the power state of each unit 100, 110, 120 is determined by analyzing the state of each unit 100, 110, 120 at the power control unit 140. The internal clock signal generator 150 then generates clock signals depending on the determined power state to drive only one of the three units 100, 110, 120. Therefore, the disclosed device is capable of performing the application program by using a driving frequency that

is about ½ to 1/3 of a conventional driving frequency so as to reduce power consumption of the audio processor.

While the teachings of the present invention have been explained in connection with particular examples, it will be apparent to those of ordinary skill in the art that the scope of this patent is not limited to those examples. On the contrary, this patent covers all structures fully within the spirit and scope of the appended claims.